What is claimed is:

1. A noise reduction device comprising:

a complementary metal-oxide semiconductor (CMOS) transistor operable as a two-terminal device in a depletion mode and having a non-linear voltage variation for charge being removed at a constant rate, the CMOS transistor is formed in an n-type substrate having an n-type drain, an n-type source, an p-type polysilicon gate, and a gate oxide layer.

2. The noise reduction device of claim 1, wherein the non-linear voltage variation is given by:

A

$$v_2(t) = Vcc - \frac{aCo}{K} - \sqrt{\left(\frac{aCo}{K}\right)^2 - \frac{2It}{K}}$$

3. The noise reduction device of claim 2, wherein the gate oxide layer has a thickness of between about twenty and forty angstroms.

Sub C1

4. A circuit comprising:

a voltage node;

a ground node; and

a transistor coupled between the voltage node and the ground node, the transistor including an p-type polysilicon gate is capable of decreasing noise signals above an absolute value of an operating voltage value at the voltage node and increasing noise signals below the absolute value of the operating voltage value.

certain capacitor capacitance in the claims

Sub C2

5. The circuit of claim 4, wherein the operating voltage value is between about .5 volts and about 1.5 volts.

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6. The circuit of claim 5, further comprising:
a logic cell coupled to the voltage node and located in close proximity to the transistor.

7. A circuit comprising:
an energy source;
a processor having a plurality of nodes coupled to the energy source and forming a power supply grid having a number of resonant frequencies; and
a number of transistors coupled to at least one of the plurality of nodes such that at least one of the number of transistors is operable as a voltage variable capacitor capable of reducing the amplitude of resonant frequencies.

8. The circuit of claim 7, wherein the number of transistors is greater than about ten thousand.

Sub C2

9. A circuit comprising:
a die having a high voltage node and a low voltage node; and
a transistor coupled between the high voltage node and the low voltage node and operable for controlling a voltage at the low voltage node.

10. The circuit of claim 9, wherein the transistor has a gate, a drain, and a source, and the gate is coupled to the high voltage node and the source and the drain are coupled to the low voltage node.

11. A circuit comprising:
a substrate;
a load fabricated on the substrate;
an energy source coupled to the load, the energy source having an operating voltage and a unidirectional noise signal; and

an electronic device fabricated on the substrate and coupled to the load, the electronic device is capable of reducing the unidirectional noise signal more than a fixed capacitor having a capacitance value equal to the capacitance value of the electronic device operating at the operating voltage.

12. The circuit of claim 11, wherein the electronic device is a voltage variable capacitor.

13. The circuit of claim 11, wherein the electronic device is a MOSFET.

Sub C3

14. A circuit comprising:

a die;

a ground node located on the die;

a voltage node located on the die; and

an electronic device coupled between the ground node and the voltage node and capable of providing an asymmetrical response to incremental voltage variations about an operational node voltage at the voltage node.

need to claim die connection

Sub E5

15. The circuit of claim 14, wherein incremental voltage variations of one polarity are damped and incremental voltage variations of the opposite polarity are amplified.

Sub C4

16. The circuit of claim 14, wherein the bias node voltage is about 1.3 volts.

voltage

17. An integrated circuit comprising:

a die;

a processor having a plurality of cells formed on the die; and

a number of electronic devices coupled to at least one of the plurality of cells and capable of damping positive voltage variations at the cell and amplifying negative voltage variations at the cell.

18. The integrated circuit of claim 17, wherein the plurality of cells are fabricated using a complementary metal-oxide semiconductor manufacturing process.

19. A method comprising:

receiving an energy signal having a noise component at a cell formed on a die; and

filtering the energy signal to form a filtered energy signal by decoupling the cell with a voltage variable capacitor.

20. The method of claim 19, wherein receiving an energy signal having a noise component at a cell comprises:

receiving a power supply signal at the cell.

21. The method of claim 19, wherein filtering the energy signal to form a filtered energy signal by decoupling the cell with a voltage variable capacitor comprises:

filtering the energy signal with at least one-hundred CMOS transistors operating in the depletion-accumulation region.

22. The method of claim 19, further comprising:

configuring at least one of the number of electronic devices to have a drain, a source, and a bulk connection coupled to a high voltage level and a gate coupled to a low voltage level.

23. A method comprising:

adding a number of electronic devices having a voltage variable capacitance to an electronic grid to suppress resonant frequencies in the electronic grid.

24. The method of claim 23, wherein adding a number of electronic devices comprises:

selecting an active electronic device; and

coupling the active electronic device between a high voltage level and a low voltage level at a logic cell.

25. The method of claim 23, further comprising:

locating at least one of the number of electronic devices between a logic cell and a decoupling capacitor.

26. A method comprising:

transforming a resonant frequency on a power supply grid network resonant at the resonant frequency to a higher frequency.

27. The method of claim 26, wherein transforming a resonant frequency on a power supply grid network resonant at the resonant frequency to a higher frequency comprises:

adding a voltage variable capacitor to the power supply grid network.

28. The method of claim 27, further comprising:

adding a plurality of CMOS transistors configured to operate in the depletion-accumulation region to the power supply grid network.